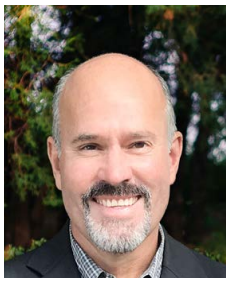

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Eutectic Die Attach Optimizes High Power GaN Devices

by Casey Krawiec, Vice President of Global Sales, StratEdge Corporation

Gallium nitride (GaN) is widely used in applications for high-power devices operating at high frequencies. This is because of its ability to operate at high currents and high voltages. While much attention is given to GaN chips, what is often overlooked is the package in which the GaN device is attached and the way the chip is attached to the package. It's well known that GaN chip efficiency and reliability can be improved by creating a package environment that reduces chip-to-package junction temperatures.

GaN, especially GaN on silicon carbide (SiC), handles higher temperatures, so it allows designers to make circuits smaller. The GaN chip can produce much greater power density, but it's the job of the package to remove the heat that is generated. The goal is to increase the power output that a chip can achieve, thereby maximizing its performance. It is important to provide a more efficient way to dissipate the heat, so the chip isn't as likely to overheat and fail during normal operation.

One way to increase power is to run a chip at a cooler temperature. Devices operating at cooler temperatures last longer, have higher reliability, and perform more efficiently. The ability to perform at a higher output conserves energy, as the same amount of electricity generates greater power output and provides a cushion when operated at a normal rate. The challenge is finding a suitable package for GaN because of its higher power density and the need to dissipate the heat while maintaining maximum device performance.

A Two-pronged Approach

StratEdge began developing GaN packaging solutions in the early 2000s by creating packages specifically tailored for GaN devices and by perfecting the packaging assembly method and means of attachment. To optimize GaN device performance, a two-pronged approach was implemented:

- Create specialized packages that maximize heat removal
- Optimize the die-attach assembly technique to maximize thermal dissipation

To accomplish both, a thermally enhanced package with an extremely flat die attach surface was created and a revolutionary gold-tin (AuSn) eutectic die attach process using mechanical agitation and heat was employed. It was important to utilize commercially available materials and processes to meet package and assembly cost targets.

Package Technology for High-frequency Devices

There are many different styles of microelectronic packages. The materials, techniques, and processes used to create the package are influential in determining package performance. There are advantages and disadvantages for every packaging technology. If the device is a high-power device operating at high frequencies, however, there are fewer package choices. Common materials used in packages include hardened ceramic substrates, molded ceramic packages, and base materials with high thermal conductivity.

For high-frequency applications, ceramic substrates are usually post-fired ceramic metalized with thick film pastes. These packages are created by laser machining hardened ceramic. The accuracy of laser-machined post-fired ceramic is much tighter than what can be achieved with multilayer co-fired ceramic. The tighter tolerance on the package cavity enables the use of relatively short wire bonds in assembly, which is better for the electrical performance of the high-frequency chip. Many of the package designs have gold conductors on the ceramic. The thick-film conductors applied to the ceramic are subjected to high temperature firing. Gold germanium (AuGe) or copper silver (CuAg) braze materials are used for

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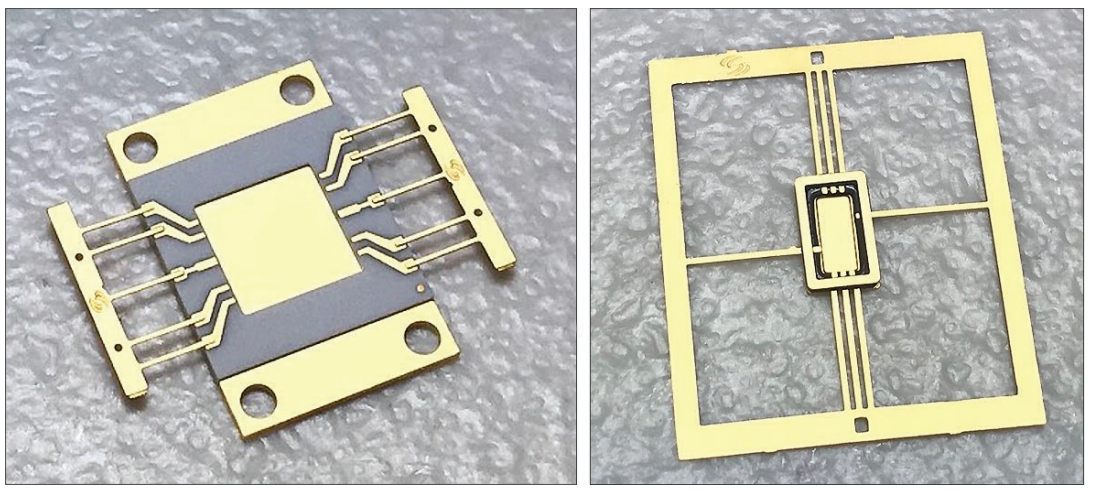

Figure 1: Examples of post-fired ceramic package with CMC base (left) and MIL-STD-hermetic molded ceramic package with CMC base (right)

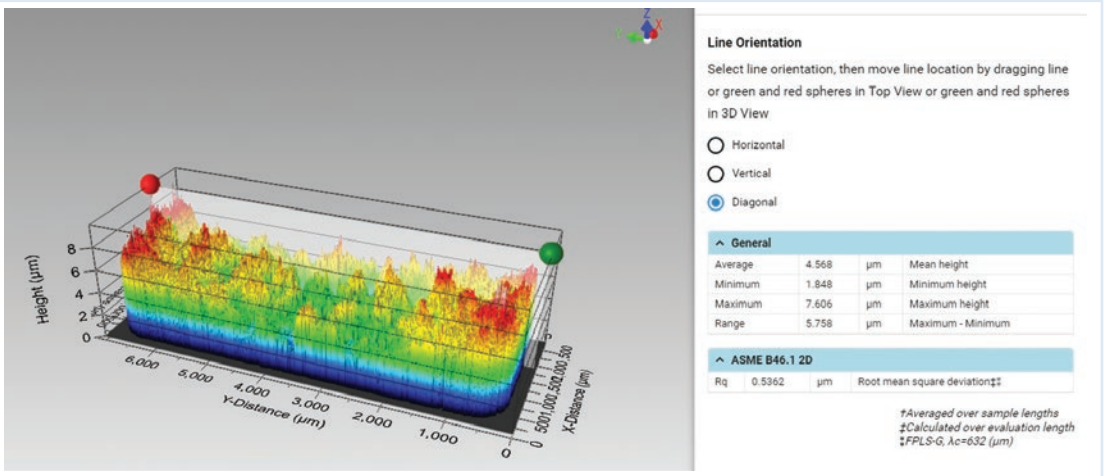

Figure 2: Spectral reflectance measurement of StratEdge package (Courtesy of Filmetrics, San Diego, CA)

attachment of the ceramic to the base material.

The high temperatures produced by GaN require a base with high thermal conductivity and a coefficient of thermal expansion (CTE) matched to the GaN device. Engineered materials like copper tungsten (CuW) composite, copper molybdenum (CuMo) composite, and laminated copper-molybdenum-copper (CMC) were developed within the industry to construct robust packages.

While copper is an excellent heat conductor with a thermal conductivity of 400 W/mK, it expands greatly when it becomes hot compared to the GaN device. Flanges made with CuW and CuMo composites combine the desirable thermal conductivity of the copper with the stiffness provided by the tungsten and molybdenum, but experimentation found that bases made with laminated layers of copper and molybdenum proved to be the best fit for GaN. Molybdenum, while not a great thermal conductor, is stiff and can be laminated to copper to provide a core that enables the entire base to have a good CTE match with the GaN device. CMC, constructed with a 1:3:1 ratio, results in an optimum balance of thermal dissipation and thermal expansion of the base material. The effective thermal conductivity in the z-direction is similar to that of CuW (15%/85%) and CuMo (10%/90%), the most commonly used copper composite base materials. What CMC provides that CuW and CuMo do not is a layer of copper directly beneath the GaN device. This enables the heat to spread away from the hot spots on the bottom of the device, which helps reduce the chip-to-package junction temperature.

Molded ceramic packages are often used when devices need to be packaged hermetically. Molded ceramic is a form of glass-to-metal seal technology where crack-resistant alumina-filled glass is used. The packages are constructed with ASTM F-15 (iron-nickel-cobalt) leads, bases, and seal rings for hermetic sealing per military standards for fine and gross leak testing. The metal surfaces have soft gold over nickel plating, which is great for gold wire bonding and AuSn eutectic die attach. If high-power GaN devices are to be packaged, commercially available high thermally conductive base materials, like CuW, CuMo, and CMC laminates are used instead of Fe-Ni-Co (iron-nickel-cobalt). As mentioned, CMC is used because the copper layer directly beneath the GaN device most efficiently spreads the heat away from the device. Examples of ceramic packages with CMC bases are shown in **Figure 1**.

In summary, packages with CMC bases that are either brazed to post-fired ceramic or brazed to a molded ceramic package using AuGe are designed specifically for high-power GaN devices. Using a flange design that has a larger volume relative to the device and is larger in x and y allows the heat to spread more rapidly. The molybdenum in the base provides a well-matched CTE by constraining the expansion of the copper. By design, the CTE of the base keeps the device in slight compression. The thermally conductive copper layer sits directly beneath the GaN device so that the heat spreads away from it immediately. By using packages with CMC bases, chip designers can take full advantage of the attributes of GaN technology.

Die Attach Assembly

StratEdge developed a proprietary AuSn eutectic die attach technique that, in conjunction with its leaded laminate (LL) packages with CMC bases, was found to achieve superior thermal dissipation. Die bonding is the process of attaching a device to a tab or heat spreader, package, or another die. AuSn eutectic die attach is a well-established method of attaching devices with AuSn solder. Both device and package must have gold on their mating surfaces. When the attachment is void-free (no gaps or pockets in the solder joint), AuSn eutectic die attach is highly reliable in performance. It's used for high reliability applications because it won't outgas and is unlikely to fail if attached properly.

There are different methods for AuSn die attach. StratEdge chose scrubbing, which is the process of heating with mechanical agitation. The die bonder used has a specially equipped stage for eutectic AuSn attachment of devices. It is an automated, highly repeatable method of scrubbing the GaN device to attach it to the package base using an 80/20 AuSn eutectic solder preform. Although AuSn is good for soldering a reliable joint, it doesn't have as high a thermal conductivity as copper. In order to maximize the thermal dissipation from the device to the package base, it is important to minimize the thickness of the AuSn solder bond line. It's the extremely thin bond line, that can only be achieved with the scrubbing process, that optimizes heat transfer. StratEdge, in partnership with die bonder equipment manufacturer Palomar Technologies, Carlsbad, CA, developed a process to ensure that achieving extremely thin bond line thicknesses of 0.00025" are routine.

The quality of the solder joint is defined by the scarcity of voids. The closer the solder joint is to being void-free, the better the reliability and thermal dissipa-

tion. To achieve the highest quality solder joint, die attach is performed using a state-of-the-art, automated scrubbing system in a class 1000 cleanroom. A solder preform is placed between the chip and die attach area of the package. The solder preforms are custom fit to the size of the die, which allows the solder volume to be minimized, thus achieving extremely thin bond lines. Precision collets (holders) are used to hold the die along its edges and, along with vacuum, secure the device tightly for accurate placement and scrubbing. The preforms and die are placed with 5-micron accuracy. Other proprietary processes are employed to minimize contamination of the surfaces so that the solder joint is as clean as possible.

One of the most important factors in the die attach process is having a base material with a smooth finish that is flat. This ensures better surface contact for attachment to the base and enhances thermal dissipation from the active device. When the die attach area is flat and smooth, the solder can flow and spread under the device more easily. The LL series packages used to develop the attachment method have a package cavity with a flatness of less than 0.001". **Figure 2** contains surface smoothness and flatness measurements made with an optical profilometer of a package with a 0.215" by 0.090" cavity. Flatness is better than 0.00017" in the area where the die is to be attached.

Another feature of these packages is that the base is attached to the package wall with virtually no braze fillet in the cavity. This is not only good for attaching to a flat, smooth surface, it also enables the device to be attached very close to the cavity wall. This allows the bond wire lengths to be shorter, which improves the performance of high-frequency devices.

As mentioned earlier, the quality of the die attach solder joint is defined by the amount of voiding in the bond line. 100% void-free bonds are desired, but that's easier said than done. MIL-STD-883 contains metrics for measuring die attach voiding using a couple of detection techniques including X-ray and ultrasonic analysis. Both require that there be at least 50% coverage with no single void being >10% of the total die attach area. In practice, one would not want a high-frequency or high-power device attachment that only meets the minimal criteria. If the largest void happens to occur under one of the transistors, degraded electrical performance due to loss of ground is possible as is overheating due to inadequate thermal dissipation. Therefore, the process needs to yield a solder joint with small and fewer voids. **Figure 3** shows a typical attachment of a GaN device with less than 4% voiding as an example of what is desirable when performing AuSn die attach.

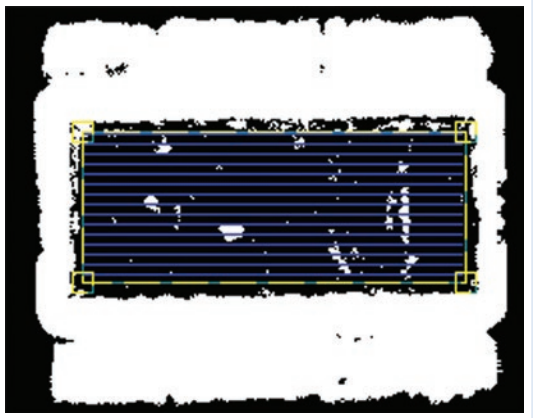

Figure 3: 96.14% solder coverage under GaN device on StratEdge LL-Series package

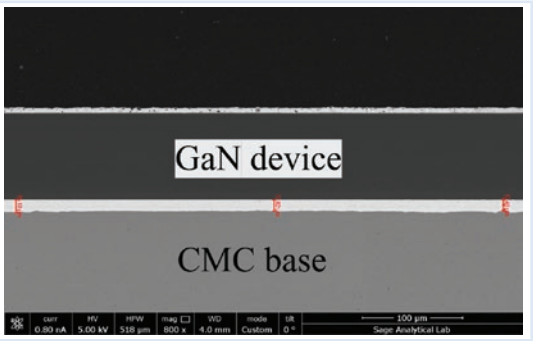

Figure 4: AuSn bond line cross section

Figure 4 shows a cross section of the packaged GaN device. The top layer is the GaN die, under which are the solder joint and the CMC base. The bond line thickness appears to be 13.15 microns, but it's actually thinner because the interface between the chip and CMC base includes chip backside metallization and nickel plating on the CMC base. Upon scrubbing, the gold dissolves into the AuSn solder joint forming the actual bond line, which is closer to 6 microns or 0.00025" thick. X-rays of the finished device assembly show minimal voiding.

Summary

The success of the eutectic attachment and the package's performance are dependent on the quality of the package construction and the type of base material of the package. The AuSn preform and custom collet are used to optimize void-free results. Using this proprietary eutectic die attach method to attach a GaN chip to a ceramic package with a CMC base has been found to drop junction temperatures by 20 degrees as compared to standard assembly methods that use ceramic packages of alternative construction. By using packages with extremely flat die attach surfaces and a AuSn eutectic die attach method that uses mechanical agitation and heat, chip temperatures are reduced, thereby improving the efficiency and reliability of the device. This results in improved device performance with increased power output and longer life for high-frequency, very high power, extremely demanding GaN devices.

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